AMENDMENTS TO THE CLAIMS:

1. (Previously Presented) A delay circuit comprising:

a delay section having two or more predetermined delay stages connected in series, each predetermined delay stage adds a predetermined delay time to a signal received by the predetermined delay stage; and

two or more selecting switch sections, wherein an input terminal thereof is connected to an output terminal of each predetermined delay stage, each selecting switch section comprises:

a selecting section means for selecting one of output terminals of the predetermined delay stages by control signal to receive a delayed input signal from the output terminal; and

a buffer section provided with first and second transistors, wherein

the delayed input signal is propagated to each gate of the first and second transistors via the selecting section means, and wherein

an output signal from the buffer section has a desired delay time.

Claims 2- 9 (Canceled)

10. (Previously Presented) The delay circuit according to Claim 35, wherein the first power supply voltage is a power supply voltage potential and the first transistor is a PMOS transistor.

11. (Previously Presented) The delay in circuit according to claim 35, wherein the second power supply voltage is a ground potential and the second transistor is an NMOS transistor.

Claims 12-17 (Canceled)

18. (Previously Presented) The delay circuit according to claim 1, wherein the rise and the fall delay time of the predetermined delay time are substantially uniform.

Claims 19-20 (Canceled)

21. (Previously Presented) The delay circuit according to claim 32, wherein each of the predetermined delay stages comprises an even number of logic inversion sections connected in series, each logic inversion section having different propagation delay time between the rise and fall transition.

22. (Previously Presented) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NAND gate, each NAND gate having the same structure, and wherein a predetermined input terminal is connected to an output terminal of preceding NAND gate.

23. (Previously Presented) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NOR gate, each NOR gate having the same structure and wherein a predetermined input terminal is connected to an output terminal of preceding NOR gate.

Claims 24-25 (Canceled)

26. (Previously Presented) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages connected in series, each predetermined delay stage adds a predetermined delay time to a signal received by the predetermined delay stage; and

two or more selecting switch sections, wherein an input terminal thereof is connected to an output terminal of each predetermined delay stage, each selecting switch sections comprises:

a selecting section means for selecting one of output terminals of the predetermined delay stages by control signal to receive a delayed input signal from the output terminal; and

a buffer section provided with first and second transistors, the delayed input signal is propagated to each gate of the first and second transistors via the selecting section means, wherein

an output signal from the buffer section has a desired delay time.

Claims 27- 31 (Canceled)

32. (Currently Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages connected in series, each ~~of which~~ delay stage is provided with a serial input terminal and an individual ~~delay~~ input terminal for inputting a signal to which predetermined delay time is added, each predetermined delay stage having substantially uniform rise delay time and fall delay time, and

selecting switch means connected to one of the individual ~~delay~~ input terminals and receiving an input signal for establishing a delay path for the input signal by selecting one of the predetermined delay stages,

wherein an output signal from the delay path has a desired delay time.

Claims 33-34 (Canceled)

35. (Previously Presented) The delay circuit according to claim 1, wherein the first transistor is connected between an output terminal outputting the output signal and a first power supply voltage, and the second transistor is connected between the output terminal and a second power supply voltage.

36. (Previously Presented) The delay circuit according to claim 1, wherein each gate of the first and second transistors is controlled by a logical gate circuit.

37. (Currently Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages connected in series, each ~~of which~~ delay stage is provided with a serial input terminal and an individual ~~delay~~ input terminal for inputting a signal to which predetermined delay time is added, each predetermined delay stage having substantially uniform rise delay time and fall delay time; and

selecting switch means connected to one of the individual ~~delay~~ input terminals and receiving an input signal for establishing a delay path for the input signal by selecting one of the predetermined delay stages,

wherein an output signal from the delay path has a desired delay time.